REMARKS

There are at least two problems with the asserted Section 102 rejection of the claims. Firstly, the language cited is simply more general than what is claimed. The general can never anticipate the specific. Thus, a *prima facie* rejection cannot possibly be made out.

The cited language is more general because it does not say anything about when a stream asserted to correspond to a logical processor is inactive. For example, it talks about a one active stream that may manipulate its own resource allocation. But there is nothing about the situation where another asserted logical processor is inactive and what you do then. Thus, plainly and incontrovertibly, the cited language is broader than the claim limitation and, because the general can never anticipate the specific, a *prima facie* rejection is not made out.

Secondly, the cited language does not meet the claim limitation that a processor execution resource previously reserved for one logical processor is made available to any of a plurality of other logical processors. This precludes one logical processor simply grabbing a resource because if the logical processor could grab it itself, then it was already available and, therefore, it was not made available "in response to a first logical processor being scheduled to enter an idle state."

For at least these two reasons, the Section 102 rejection should be reconsidered.

Similarly, the Section 103 rejection of claims 9 and 28 relies on hindsight reasoning. It simply takes the situation claimed, conceives that nothing in the single cited reference teaches it, and then concludes it would be obvious subjectively to the Examiner. But this is certainly not the test and never has been.

Therefore, reconsideration should be undertaken.

Respectfully submitted,

Date: September 27, 2011

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